IOSR Journal of Mechanical and Civil Engineering (IOSR-JMCE)
e-ISSN: 2278-1684,p-ISSN: 2320-334X,
PP 10-11
www.iosrjournals.org

Design and Modeling of Hybrid CMOS SET Based Comparator for Next Generation IC

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ABSTRACT : *A new designed structure namely Hybrid CMOS SET can conglomerate both merits of Single Electron Transistor (SET) and CMOS transistor. The authors here illustrate Hybrid CMOS SET based logic gates in designing advanced decision making Nano IC's using logic based comparator. The concept is to be incorporated in next generation electronic system and the operation is validated using Tanner environment.*
Keywords -*Hybrid CMOS SET, SET, SED.*

I. INTRODUCTION

The Single Electron Devices (SED) is considered as flourishing technology in the present day world. It has enormous features in device integration. Most of the research publications are facing the fact existing CMOS that ranges in 100nm will be forced to share its present dominance with SET's in the next generation IC design although CMOS and SET's [1-3]are relatively converse in nature.

SET by nature is a low-power consuming device which demonstrates higher speed and robustness along with high integration density like advanced new functionalities. On the other side CMOS possess unbeatable characteristics like high voltage gain no background charge. Thus CMOS is blessed to compensate exactly the intrinsic limitations of SETs. Evidently hybridizing of SET and CMOS is likely to have emerged with new functionalities in the next generation device technology. To exploit SET to function as a switch it is customary to push the SET into the Coulomb blockade state i.e., the "OFF" condition and accordingly channel it to conduct current i.e., the "ON condition. Once it is done, it becomes ready to work like a MOSFET logic realization to model a hybrid CMOS-SET logic family. The straight forward design approach is that the hybrid CMOS-SET threshold logic is formed by a PMOS transistor as the load resistance of an SET. However these devices has PMOS transistor connected as a load to the SET which is typically distinct from any other evolved post CMOS devices. Thus some design rules has been set by Researchers and that is exclusively implied before practical hybrid CMOS-SET [4-6] circuit demonstration. However the concept of hybrid CMOS-SET modeling is in its elementary stage but even then empirical studies had been initiated by the Researchers. The authors here limited themselves in incorporating this new technology as a decision making tool.

II. MODUS OPERANDI

A comparator is a logic device used to compare the magnitudes of two binary numbers. Depending on the design, it may either simply provide an output that is active (goes HIGH) when two numbers are equal or additionally provide outputs that signify which of the numbers is greater when equality does not hold.

The XNOR gate is the basic comparator because its output is 1 only if its two input bits are equal that is output is a 1 if and only if the input bits coincide. Two binary numbers are equal, if and only if all their corresponding bits coincide. However it is obvious that this circuit can be expanded or compressed to accommodate binary numbers with any number of bits. The block diagram of comparator which can be used as a module for comparison is shown in Fig.1. If A=1 B=0 then A>B. Therefore A>B:G=AB' . If A=0 B=1 then A<B. Therefore A<B:L=A'B. If A and B coincide then A=B. Therefore A=B:E=AΘB[14-18].

III. FIGURE

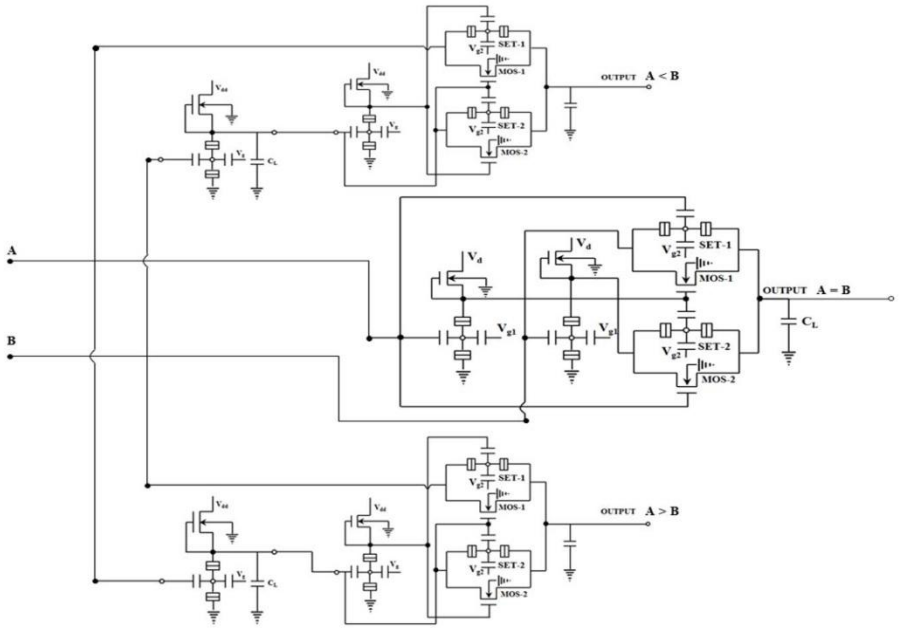

Fig1: Hybrid CMOS SET based Comparator

IV. CONCLUSION

Designing Hybrid CMOS SET comparator has been illustrated in this short communication using hybrid CMOS SET logic gates. The authors aim to implement this as a decision making tool. Computer simulations revealed perfect logical operations of designed circuit. The intensification of such research has undoubtedly enhanced and it now requires potential contribution from all fields of electronic research.

ACKNOWLEDGEMENTS

The authors acknowledge sincerely Prof.(Dr.) JayantaGope for his continuous support and help.

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